

Docket No.: 08211/0200347-US0/P05786

(PATENT)

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Ols Hidri et al.

Application No.: 10/695,921

Confirmation No.: 7033

Filed: October 28, 2003

Art Unit: 2838

For: GENERATING REFERENCE VOLTAGES

Examiner: A. D. Berhane

## **INFORMATION DISCLOSURE STATEMENT (IDS)**

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action after the filing of a Request for Continued Examination under 37 CFR 1.114 (37 CFR 1.97(b)(4)).

A copy of only those documents listed below is attached:

## **Other Documents**

BUCK et al., "A CMOS Bandgap Reference Without Resistors", IEEE Journal of Solid-State Circuits, Vol. 37, No. 1, pp. 81-83, January 2002.

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In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Commissioner is authorized to charge any deficiency of up to \$300.00 or credit any excess in this fee to Deposit Account No. 04-0100.

Dated: December 5, 2005

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PTO/SB/08a/b (07-05) Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1449A/B/PTO				Complete if Known		
				Application Number	10/695,921-Conf. #7033	
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l s	TATEMENT B	3Y /	APPLICANT	First Named Inventor	Ols Hidri	
				Art Unit	2838	
	(Use as many sheets as necessary)			Examiner Name	A. D. Berhane	
Sheet	1	of	1	Attorney Docket Number	08211/0200347-US0/P05786	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	Document Number  Number-Kind Code <sup>2</sup> ( if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	Foreign Patent Document  Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> ( <i>if known</i> )	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>		
	CA	BUCK et al., "A CMOS Bandgap Reference Without Resistors", IEEE Journal of Solid-State Circuits, Vol. 37, No. 1, pp. 81-83, January 2002.			

<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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